UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/751,432	12/29/2000	Walter L. Snyder	ITL.1518US (P9714)	7648

21906 7590 07/19/2007

TROP PRUNER & HU, PC
1616 S. VOSS ROAD, SUITE 750
HOUSTON, TX 77057-2631

EXAMINER	
MEONSKE, TONIA L	
ART UNIT	PAPER NUMBER
2181	

MAIL DATE	DELIVERY MODE
07/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

80

Office Action Summary	Application No.	Applicant(s)	
	09/751,432	SNYDER ET AL.	
	Examiner	Art Unit	
	Tonia L. Meonske	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 8-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 27 is objected to because of the following informalities:

In line 2, please change "of" to "on". Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) a patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-4, 8-13, 16-17 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cloutier, US Patent 5,892,962 (herein after Cloutier), in view of Taylor et al., US Patent 5,603,043 (herein after Taylor), and Bartlett et al., US Patent 3,662,349 (herein after Bartlett).

4. Referring to claim 1, Cloutier has taught a re-targetable communication processor, comprising:

a. a connectivity unit (Figure 1, element 106);

b. a digital signal processing core coupled to the connectivity unit (Figure 1, element 104, one of the FPGA's is a digital signal processor);

c. a plurality of scaleable functional units, coupled to the connectivity unit, to execute mathematically intensive operations (Figure 1, element 104, column 1, lines 32-36), further including:

1. a local memory (Figure 1, elements 11 and 112);

11. a plurality of complex arithmetic elements (hereinafter CAE) coupled to one another (Figure 1, element 104) and to an inter-CAE bus (Figure's 1 and 2, element 114), each of the plurality of CAEs to access the local memory (Figure 1, column 2, lines 26-43, Each CAE, element 104 in element 102, accesses local memory, elements 110 and 112, through processes controller element 108.) and including a CAE memory (Figure 1, element 120), and an arithmetic unit (abstract, column 2, lines 9-16, column 2, line 62-column 3, line 14, Each CAE has a dynamic arithmetic unit.); and

111. a bus controller coupled to the inter-CAE bus and the connectivity unit (Figure 1, element 106).

5. Cloutier has not taught a plurality of removable complex arithmetic elements. However, Taylor has taught a plurality of removable complex arithmetic units (column 8, lines 35-55, column 10, lines 15-19) for the desirable purpose being able to update the system with faster parts or parts with more resources as needed. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the complex arithmetic units of Cloutier, be removable, as taught by Taylor, for the desirable purpose of being able to update the system with faster parts or parts with more resources as needed (column 8, lines 35-55, column 10, lines 15-19).

6. Cloutier has not taught that each of the plurality of CAEs includes a sequencer to cause data to be sequenced from the CAE memory to only the arithmetic unit and to cause only the arithmetic unit to execute an operation on the data and to cause only the arithmetic unit to execute an operation on the data. However, Bartlett has taught that having separate sequencers would have decreased the number of bits per sequencer over that of a single sequencer. Decreasing the number of bits per sequencer simplifies decoding. (Bartlett, column 2, lines 20-60) Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have each of the plurality of CAE's include a sequencer (instead of just the single centralized sequencer of Cloutier, Figure 1, element 108) to cause data to be sequenced from a CAE memory to only the arithmetic unit and to cause only the arithmetic unit to execute an operation on the data and to cause only the arithmetic unit to execute an operation on the data, for the desirable purpose of simplifying decoding and efficiently and independently executing the arithmetic tasks.

7. Referring to claim 2, Cloutier has taught the re-targetable communication processor according to claim 1, as described above, and the plurality of CAEs further comprising:

a. the CAE memory to store data for the mathematically intensive operations (Figure 1, element 120);

b. a data router coupled to the CAE memory (FPGA's inherently contain data router to route data);

c. the arithmetic unit, coupled to the CAE memory and the data router, to execute operations in accordance with the control information (abstract, column 2, lines 62-67, column 3, lines 33-39); and

d. the data router to route data to the sequencer and the CAE memory and to facilitate communications among the CAEs in the scaleable functional unit (Figure 2, The data router inherently routes data to the devices over, north, south, east, west, 114, 1 18, and data lines.).

8. Referring to claim 3, Cloutier has taught the re-targetable communication processor according to claim 2, as described above, and the CAE memory further comprising: two banks of separately addressable data memories (Figure 1, Each memory is separately addressable.).

9. Referring to claim 4, Cloutier has taught the re-targetable communication processor according to claim 3, as described above, and the arithmetic unit further comprising:

a. a register file to accept data from the data memories (column 2, lines 53-61, column 3, lines 15-22); and

b. a plurality of multiplier-accumulator engines, coupled to one another, to the register file and to the data memories, to operate on the mathematically intensive operations (column 8, lines 56-59).

10. Referring to claim 8, Cloutier has taught the re-targetable communication processor according to claim 1, as described above, and further including a micro-controller core coupled to the connectivity unit (Figure 1, element 108).

11. Referring to claim 9, Cloutier has taught the re-targetable communication processor according to claim 2, as described above, and wherein a first delay introduced by the sequencer is to match a second delay introduced by the arithmetic unit (FPGAs inherently run in lock step with the controller, or sequencer.).

12. Claim 10 has nothing over claim 1 and is therefore rejected for the same reasons as set forth in claim 1.

13. Claim 11 has nothing over claim 2 and is therefore rejected for the same reasons as set forth in claim 2.

14. Claim 12 has nothing over claim 3 and is therefore rejected for the same reasons as set forth in claim 3.

15. Claim 13 has nothing over claim 4 and is therefore rejected for the same reasons as set forth in claim 4.

16. Claim 16 has nothing over claim 2 and is therefore rejected for the same reasons as set forth in claim 2.

17. Claim 17 has nothing over claim 9 and is therefore rejected for the same reasons as set forth in claim 9.

18. Referring to claim 27, Cloutier has taught the re-targetable communication processor according to claim 1, as described above. Cloutier has not specifically

taught wherein the re-targetable communication processor is formed of a single integrated circuit. However, Official Notice is taken that a processor being formed on a single integrated circuit requires less circuitry and speeds up overall system communication. Going off chip for information is extremely slow. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the re-targetable communication processor of Cloutier, Taylor and Bartlett be formed of a single integrated circuit, for the desirable purpose of simplifying the circuitry and speeding up overall system communications.

19. Claims 5, 6, 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cloutier, US Patent 5,892,962 (herein after Cloutier), in view of Taylor et al., US Patent 5,603,043 (herein after Taylor), Morton, US Patent 6,088,783 (herein after Morton), and Bartlett et al., US Patent 3,662,349 (herein after Bartlett).

20. Referring to claim 5, Cloutier has taught the re-targetable communication processor according to claim 4, as described above. Cloutier has not taught the multiplier-accumulator engine further comprising: a. a pre-adder to generate a first sum by adding data from the register file and the data memory; b. a multiplier to generate a multiplier output by multiplying data from the data memories or the first sum; c. an accumulator to generate a second sum by adding the multiplier output or data from the data memories; and d. a data packing block to configure the second sum into a pre-defined format.

21. However, Morton has taught the multiplier-accumulator engine further comprising:

a. a pre-adder to generate a first sum by adding data from the register file and the data memory (Figure 8, element 809);

b. a multiplier to generate a multiplier output by multiplying data from the data memories or the first sum (Figure 8, element 812);

c. an accumulator to generate a second sum by adding the multiplier output or data from the data memories (figure 8, element 812); and

d. a data packing block to configure the second sum into a pre-defined format (Column 25, line 59-column 26, line 23, 16-bit portions).

22. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the multiplier-accumulator engine of Cloutier, be configured like that of Morton, as described above, for the desirable purpose of allowing quick multiply/accumulate operations on the data (Column 25, line 59-column 26, line 23).

23. Referring to claim 6, Cloutier has taught the re-targetable communication processor according to claim 5, as described above, and the multiplier further including a programmable shifter (column 8, lines 52-57).

24. Claim 14 has nothing over claim 5 and is therefore rejected for the same reasons as set forth in claim 5.

25. Claim 15 has nothing over claim 6 and is therefore rejected for the same reasons as set forth in claim 6.

26. Claims 18-21 and 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cloutier, US Patent 5,892,962 (herein after Cloutier), in view of Taylor et al., US Patent 5,603,043 (herein after Taylor), Treiber et al., US Patent 6,324,062 (herein after Treiber), and Bartlett et al., US Patent 3,662,349 (herein after Bartlett).

27. Referring to claim 18, Cloutier has taught a computer system, comprising:

a. a microprocessor (Column 2, lines 39-44, Host) coupled to a system bus (Figure 1, element 122);

b. a system controller coupled to the system bus (Column 2, lines 39-44); and

c. an input/output controller hub (Figure 1, element 106), coupled to the system controller and coupled to an input/output bus (Figure 2, element 114);

d. and coupled to the input/output bus, further including:

e. a re-targetable communication system formed on a single integrated circuit (column 1, lines 25-64), comprising:

i. a connectivity unit (Figure 1, element 106);

ii. a digital signal processing core coupled to the connectivity unit (Figure 1, element 104, one of the FPGA's is a digital signal processor);

iii. a plurality of scaleable functional units, coupled to the connectivity unit, to execute mathematically intensive operations (Figure 1, element 104), further including:

(1) a local memory (Figure 1, elements 11 and 112);

(2) a plurality of complex arithmetic elements (hereinafter CAE) coupled to one another (Figure 1, element 104) and to an inter-CAE bus (Figures 1 and 2, element 1 14), each of the plurality of CAEs to access the local memory (Figure 1, column 2, lines 26-43, Each CAE, element 104 in element 102, accesses local memory, elements 110 and 112, through processes controller element 108.) and including a CAE memory (Figure 1, element 120), and an arithmetic unit (abstract, column 2, lines 9-16, column 2, line 62-column 3, line 14, Each CAE has a dynamic arithmetic unit.); and

(3) a bus controller coupled to the inter-CAE bus and the connectivity unit (Figure 1, element 106).

iv. a media access control processor coupled to the connectivity unit (column 4, lines 20-34, optical scanner)

28. Cloutier has not taught a plurality of removable complex arithmetic elements. However, Taylor et al. have taught a plurality of removable complex arithmetic units (column 8, lines 35-55, column 10, lines 15-19) for the desirable purpose being able to update the system with faster parts or parts with more resources as needed. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the complex arithmetic units of Cloutier, be removable, as taught by Taylor et al., for the desirable purpose of being able to update the system with

faster parts or parts with more resources as needed (column 8, lines 35-55, column 10, lines 15-19);

29. Cloutier has not taught that the re-targetable communication system is an add-in card. However, Treiber has taught a processor system that is removable so that the system does not have to be powered down while swapping out a part, thereby enabling hot swapping (abstract, column 8, lines 10-14). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the re-targetable communication system of cloutier be implemented as an add in card, for the desirable purpose of allowing hot swapping to occur without an overall system power down.

30. Futhermore, Cloutier has not taught that each of the plurality of CAEs includes a sequencer to cause data to be sequenced from a CAE memory to only the arithmetic unit and to cause only the arithmetic unit to execute an operation on the data. However, Bartlett has taught that having separate sequencers would have decreased the number of bits per sequencer over that of a single sequencer. Decreasing the number of bits per sequencer makes decoding much simpler. (Bartlett, column 2, lines 20-60) Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have each of the plurality of CAE's include a sequencer (instead of just the single centralized sequencer of Cloutier, Figure 1, element 108) to cause data to be sequenced from a CAE memory to only the arithmetic unit and to cause only the arithmetic unit to execute an operation on the data, for the desirable purpose of

simplifying decoding and efficiently and independently executing the arithmetic tasks.

31. Furthermore, Cloutier has not specifically taught wherein the re-targetable communication processor is formed on a single integrated circuit. However, Official Notice is taken that a processor being formed on a single integrated circuit requires less circuitry and speeds up overall system communication. Going off chip for information is extremely slow. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the re-targetable communication processor of Cloutier, Taylor, Treiber and Bartlett be formed of a single integrated circuit, for the desirable purpose of simplifying the circuitry and speeding up overall system communications.

32. Claim 19 has nothing over claim 2 and is therefore rejected for the same reasons as set forth in claim 2.

33. Claim 20 has nothing over claim 3 and is therefore rejected for the same reasons as set forth in claim 3.

34. Claim 21 has nothing over claim 4 and is therefore rejected for the same reasons as set forth in claim 4.

35. Claim 24 has nothing over claim 7 and is therefore rejected for the same reasons as set forth in claim 7.

36. Claim 25 has nothing over claim 8 and is therefore rejected for the same reasons as set forth in claim 8.

37. Claim 26 has nothing over claim 9 and is therefore rejected for the same reasons as set forth in claim 9.

38. Claims 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cloutier, US Patent 5,892,962 (herein after Cloutier), in view of Taylor et al., US Patent 5,603,043 (herein after Taylor), Treiber et al., US Patent 6,324,062 (herein after Treiber), Morton, US Patent 6,088,783 (herein after Morton), and Bartlett et al., US Patent 3,662,349 (herein after Bartlett).

39. Claim 22 has nothing over claim 5 and is therefore rejected for the same reasons as set forth in claim 5.

40. Claim 23 has nothing over claim 6 and is therefore rejected for the same reasons as set forth in claim 6.

Response to Arguments

41. Applicant's arguments with respect to claims 1, 10 and 18, on page 9, lines 12-23 and on page 10, lines 3-9 have been considered but are moot in view of the new ground(s) of rejection.

42. Applicant's arguments filed with respect to claim 1 have been fully considered but they are not persuasive.

43. On pages 9 and 10, Applicant argues in essence:

> *"The rejection of claim 1 is improper as there is no basis for combining, at least, Bartlett with the remaining references. In this regard, Bartlett is directed to a program system for a telephone exchange. Bartlett adds no teaching with regard to the claimed subject matter; not are the sequencers in Bartlett each associated with a separate arithmetic unit to cause data to be sequenced from an associated memory to only the arithmetic unit and to cause only the arithmetic unit to execute an operation on the data sequenced."*

However, in response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Bartlett has been merely cited for teaching the concept of having separate sequencers, instead of a single centralized sequencer. Bartlett has further taught that having separate sequencers would have decreased the number of bits per sequencer over that of a single sequencer, which simplifies decoding. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have each of the plurality of CAE's of Cloutier include a sequencer (instead of just the single centralized sequencer of Cloutier, Figure 1, element 108) to cause data to be sequenced from a CAE memory to only the arithmetic unit and to cause only the arithmetic unit to execute an operation on the data and to cause only the arithmetic unit to execute an operation on the data, for the desirable purpose of simplifying decoding and efficiently and independently executing the arithmetic tasks. Therefore this argument is moot.

44. On page 10, Applicant argues in essence:

"While not described further herein, dependent claims standing rejected over combinations including five or more references cannot stand for the further reason that there is absolutely no basis or motivation for combining these numerous references from disparate fields to obtain the subject matter of the dependent claims."

However, in response to applicant's argument that the examiner has combined an excessive number of references, reliance on a large number of references in a rejection does not, without more, weigh against the obviousness of the claimed invention. See *In re Gorman*, 933 F.2d 982, 18 USPQ2d 1885 (Fed. Cir. 1991). Therefore this argument is moot.

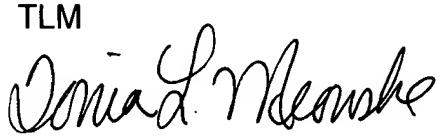
Conclusion

45. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday with first Friday's off.

46. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

47. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TLM



Tonia L. Meonske
July 16, 2007